In re Patent Application of:
FRANCIS ET AL.
Serial No. **10/008,586**
Filing Date: **NOVEMBER 5, 2001**

REMARKS

The Applicants would like to thank the Examiner for the thorough examination of the present application.

Independent Claims 12, 20 and 31 have been amended to more clearly define the present invention over the cited prior art references. In particular, independent Claim 12 has been amended to include the subject matter from dependent Claim 17 and intervening Claim 14; independent Claim 20 has been amended to include the subject matter from dependent Claim 24 and intervening Claim 22; and independent Claim 31 has been amended to include the subject matter from dependent Claim 36 and intervening Claim 33. Dependent Claims 14, 17, 22, 24, 33 and 36 have been cancelled and the dependency of certain other dependent claims has been changed for consistency.

The claim amendments and arguments supporting patentability of the claimed invention are presented below.

I. The Claims Are Patentable

The Examiner rejected independent Claims 12, 20 and 31 over the Smith patent. Since the independent claims have been amended to include the subject matter from certain dependent claims as stated in the Remarks, the rejection of these claims will be discussed based upon the rejection of Smith in view of Matoba. Independent Claim 26 will also be discussed along with the rejection of amended independent Claims 12, 20 and 31.

The present invention, as recited in amended independent Claim 12, for example, is directed to a system-on-chip (SOC) comprising a plurality of circuit blocks, each

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responsive to a respective local clock signal, and at least one system clock connected to the circuit blocks for providing a system clock signal thereto for functioning as the respective local clock signals. A power control manager is connected to the circuit blocks via respective clock enable lines for selectively providing a shutdown signal thereto. The power control manager comprises at least one register connected to the respective clock enable lines for storing data indicating logic states of the shutdown signals. Each circuit block comprises a local power control circuit for selectively maintaining the system clock signal as the local clock signal even after receiving the shutdown signal if the circuit block is in an active state when the shutdown signal is received.

An advantage of the present invention is that the shutdown circuit in each circuit block allows the circuit block to be safely shutdown after receiving the shutdown signal. It can be difficult to establish an exact time when it is possible to switch off the clock to a circuit block without causing errors. In some cases, if the clock to the circuit block is stopped abruptly, there is a risk of preventing a critical operation of the circuit block from being carried out. For example, a circuit block could be performing a necessary communication protocol and the shutdown of the block could cause the SOC to disregard the protocol. Examples of protocols that could easily be disregarded include memory-DMA, and master-slave blocks among others. Additionally, removing a system clock from a counter or a timing signal generator could be fatal to that particular circuit block..

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Amended independent Claim 20 is similar to amended independent Claim 12 except this claim recites a clock signal instead of a local clock signal, and each circuit block further comprises a block logic circuit providing a status signal indicating whether the circuit block is in an active or idle state. Amended independent method Claim 31 is similar to amended independent device Claim 12.

Independent Claim 26 is similar to independent Claim 12 except this claim recites a clock signal instead of a local clock signal, and further recites a central processing unit connected to the power control manager for determining whether each circuit block is in an active or idle state by querying the at least one register.

Referring now to Smith and to FIG. 1 in particular, the Examiner characterized the illustrated integrated circuit as a system-on-chip (SOC) comprising a plurality of circuit blocks **11-14**, a system clock connected to the circuit blocks for providing a system clock signal **35** thereto, and a power control manager **1** connected to the circuit blocks for selectively providing a shutdown signal **15-18** thereto. The Examiner characterized each circuit block **11-14** as comprising a shutdown circuit (NAND gates **27-30** and **44-47**, flip-flops **23-26** and inverters **36-39**) for preventing the system clock signal **35** from functioning as the respective local clock signal based upon the shutdown signal.

The Examiner correctly acknowledges that Smith fails to disclose at least one register in the power control manager **1** for storing data indicating logic states of the shutdown signals for the current blocks **11-14**. The Examiner cited Matoba as disclosing this feature. FIG. 1 of Matoba discloses

a power control manager **15** comprising a register **16a** connected to respective clock enable lines **INTR0-INTR3** for storing data indicating logic states of the shutdown signals.

The Examiner somehow makes the leap that since Smith discloses a power control manager **1** connected to the circuit blocks **11-14** for selectively providing a shutdown signal **15-18** thereto, it would have been obvious to modify the power control manager **1** to include at least one register for storing data indicating logic states of the shutdown signals. Applicants respectfully disagree and assert that there is no proper motivation to modify the Smith patent in the manner set forth by the Examiner. Absent the Applicants' disclosure, one of ordinary skill in the art would not look to modify the power control manager **1** as illustrated in FIG. 1 of Smith to include a register as disclosed in Matoba.

Instead, Smith teaches away from using a register in the power control manager **1**. The power control manager **1** operates in response to the addresses received on the system bus **9**, and based upon a comparison of the addresses by the comparison circuitry **2**. Reference is directed to column 2, lines 53-67 of Smith, which provides:

> "The central arbiter **1** and the comparison circuitry **2** monitor the system bus **9** for addresses within the range controlled by the central arbiter **1** and for specific corresponding commands, whose completion will require the operation of this electronic system or integrated circuit. When an address within the controlled range and a specific corresponding command is detected, the central arbiter **1** then determines which functional blocks **11-14**

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> will be necessary for completion of its task. Once the central arbiter **1** determines which functional blocks **11-14** will be required for operation, the central arbiter **1** pulls the respective Start_Clock signal lines **15-18** to a logical low voltage level, causing the output of the respective NAND gates **44-47** to switch from a logical low voltage level to a logical high voltage level." (Emphasis added.)

Reference is also directed to column 3, lines 13-20 of Smith, which provides:

> "The system bus **9** is coupled as an input to the central arbiter **1**. The central arbiter **1** is coupled to the comparison circuitry **2** through the address lines **7** which provide the address from the system bus **9** to the comparison circuitry **2**. The comparison circuitry **2** is also coupled to the central arbiter **1** through the control line **8** which informs the central arbiter **1** when the address on the address lines **7** is in the range of addresses controlled by the central arbiter **1**." (Emphasis added.)

The power control manager **1** thus operates in response to the comparison circuitry **2**. When an address received by the system bus **9** is within a range of an address controlled by the power control manager **1**, then the power control manager **1** will provide a shutdown signal to the circuit blocks **11-14**. Instead of storing the logic states of the shutdown signals in the power control manager **1**, the power control manager **1** continuously monitors the system bus **9**. (Column 7, lines 10-14 of Smith.) Upon detecting that the system needs to transmit or receive signals, the power control

manager **1** re-enables the clock signal to the circuit blocks **11-14** which are required for the transmission or reception. Smith thus fails to make any reference to the logic states of the respective clock enable signals being stored in the power control manager **1**.

Applicants thus assert that only in hindsight, and having the benefit of the Applicants' disclosure, would the skilled artisan possibly be motivated to modify the power control manager **1** in Smith to include a register as disclosed in Matoba. In other words, one skill in the art would not look to modify Smith absent having the benefit of studying the Applicants' disclosure.

Therefore, the Applicants submit that amended independent Claim 12 is patentable over Smith in view of Matoba. Amended independent Claims 20 and 31 and independent Claim 26 are similar to amended independent Claim 12, and it is submitted that these claims are also patentable over Smith in view of Matoba. In view of the patentability of independent Claims 12, 20, 26 and 31, their respective dependent claims, which recite yet further distinguishing features, are also patentable, and require no further discussion herein.

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CONCLUSION

In view of the amendments to the claims and the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number 703-872-9306 to the Commissioner for Patents on this 8th day of November, 2004.

Michael W. Taylor